COMMON PROBLEMS IN PCB DESIGN

BASED ON MINT-TEK CIRCUITS EXPERIENCE OF
DESIGNSPARK

MINT-TEK.COM

ISSUE 1

UNNECESSARY INFORMATION

ISSUE 1.1

THE MANUFACTURER DOES NOT RECOGNISE THE FUNCTION OF THESE LAYERS.

Result: Unnecessary delay while the manufacturer asks for clarification.

In this case, the engineer has extracted the manufacturing data from his CAD package and sent on all the information without actually taking the time to look at it, and only sending the necessary information.

The manufacturer has a duty to view all the information it receives and will query any extra information, causing unnecessary delays to the production process

Geber files needed for manufacture are:

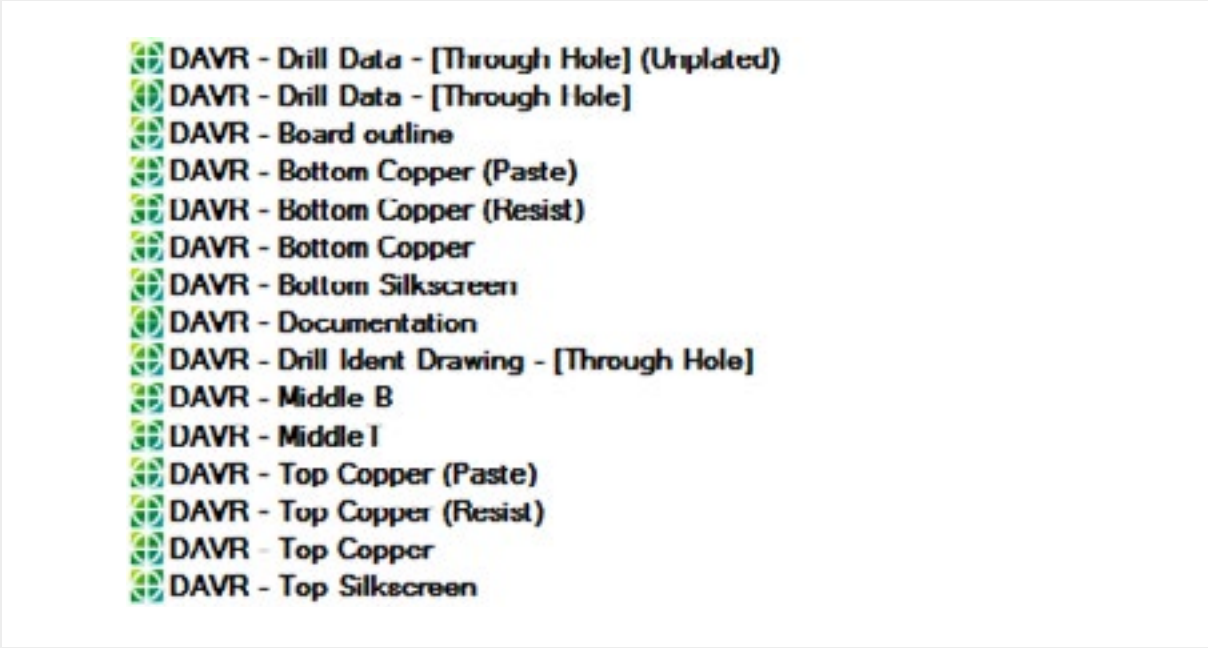
LAYER	FILE EXT IN DESIGN SPARK
Top	GBR
Inner	GBR
Bottom	GBR
Top Mask	GBR
Bottom Mask	GBR
Top Silk	GBR
Bottom Silk	GBR
Top Paste	GBR
Bottom Paste	GBR
Board Outline	GBR
Drill	DRL

ISSUE 2

INSUFFICIENT INFORMATION

ISSUE 2.1

THERE IS NO SPECIFICATION OF THE LAYER SEQUENCE.



Result: Unnecessary delay while the manufacturer asks for clarification.

In this example the inner layers are labelled “Middle T” and “Middle B”. The designer may think this makes total sense - that “Middle T” would go next to the top layer and “Middle B” next to the bottom. Manufacturers don’t assume unless they are familar with your work and have previously seen the same layer configuration.

More than likely they will place the order on hold and query it.

ISSUE 2.2

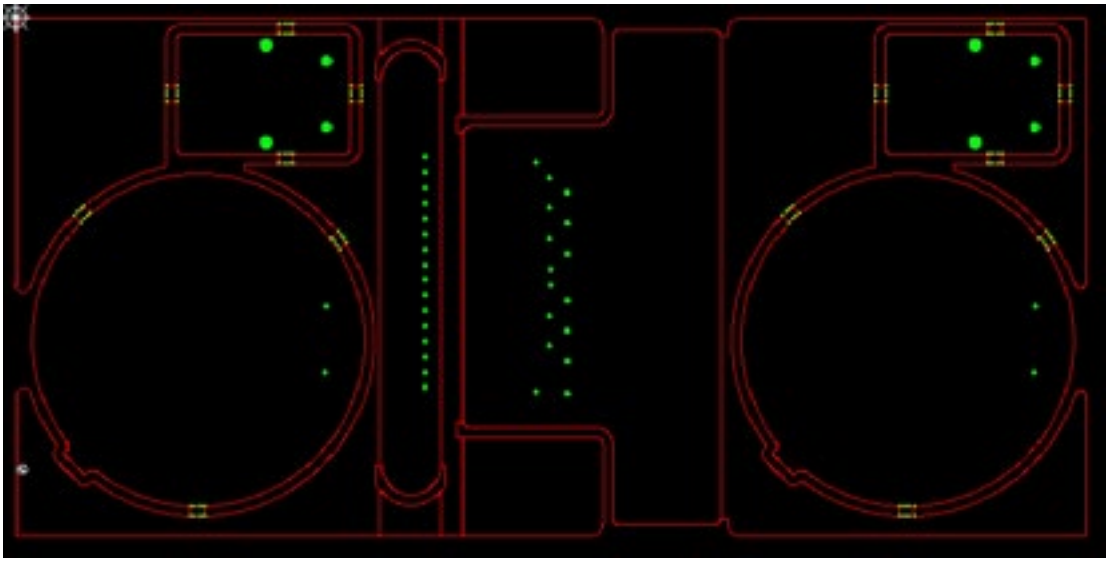
MANUFACTURER DOESN’T RECOGNISE OR UNDERSTAND THE FUNCTION OF A FILE.

Result: Unnecessary delay while the manufacturer asks for clarification.

In this case, the designer has sent extra information with no clarification on its purpose. Again, the manufacturer will seldom make assumptions and will have to get more information.

ISSUE 2.3

THERE IS NO CLEAR DESCRIPTION ON HOW TO SEPERATE PCBS ON MULTIPLE BOARD PANELS.



Result: Unnecessary delay while the manufacturer asks for clarification.

In order to reduce cost, users will often combine PCBs on one panel. It takes a little bit of planning but can be quite successful for a good designer. Often, the designer does not specify how the boards will be held in the panels. Without specifying, they will be held with pips and stamp holes. There are other options.

ISSUE 3

CONFLICTING INFORMATION

ISSUE 3.1

OUTLINE OF THE BOARDS.

fig. 1

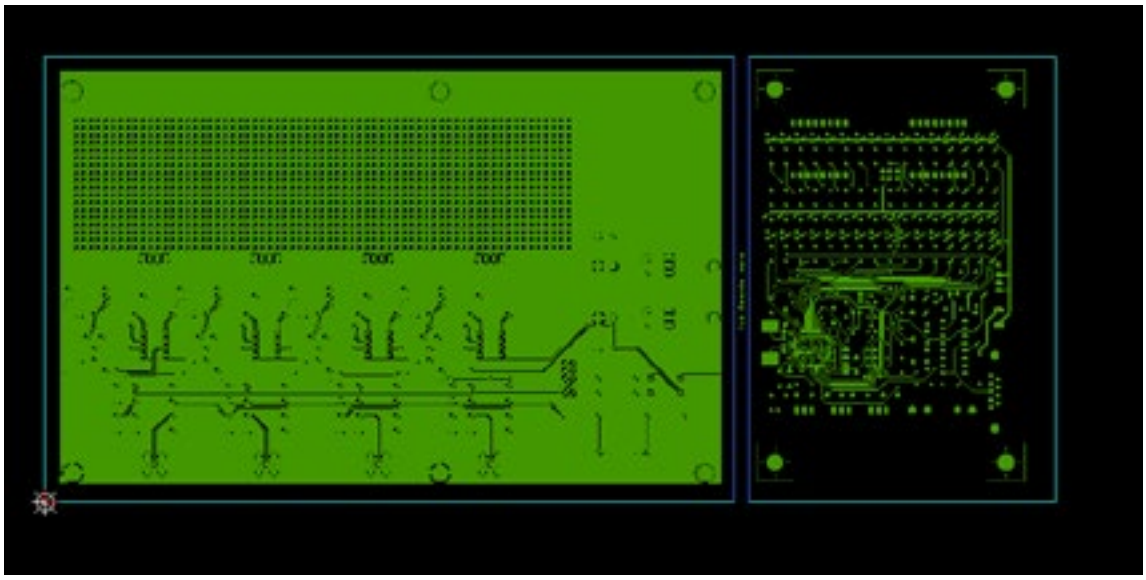
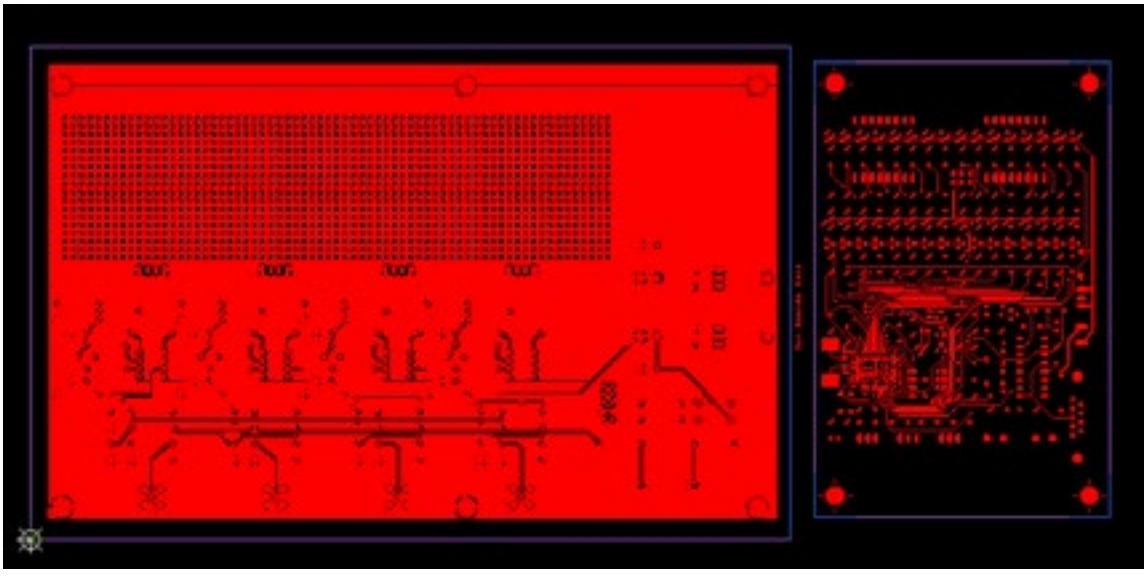


fig. 2



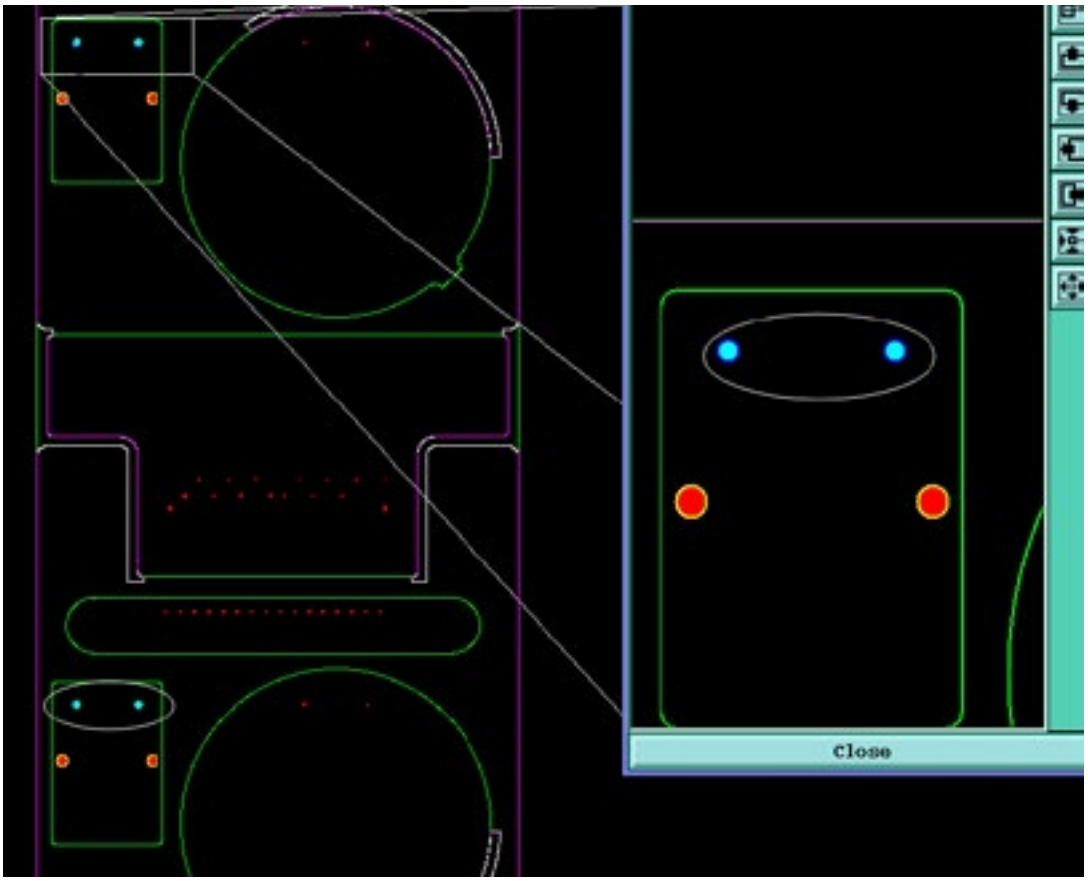
Result: Unnecessary delay while the manufacturer asks for clarification.

The customer has supplied a board outline layer which clearly details the outlines for two separate boards. On the top layer of the smaller board you can see that there are what appear like corner markers left inside the board. *fig. 1*

This conflicts with the outline in the contour layer, shown in **fig. 2**. The PCB manufacturer will not make any assumptions here and will delay approval for production until it is cleared up. Layout Engineers should remove any ambiguous notations from the outline or add a note with an explantation and instructions for how to deal with them.

ISSUE 3.2

CIRCUIT PADS IN OUTLINE HAVE NO CORRESPONDING INFORMATION ON OTHER LAYERS.



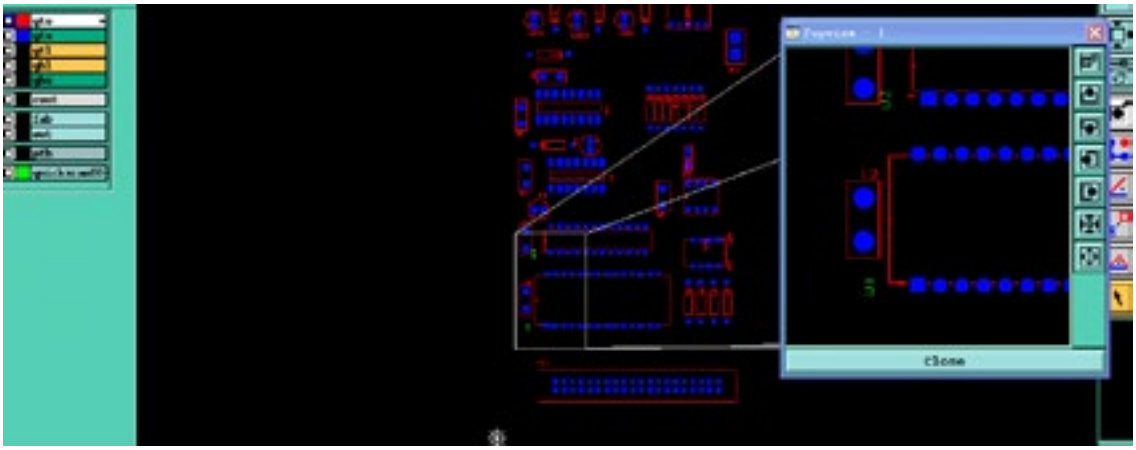
Result: Unnecessary delay while the manufacturer asks for clarification.

A very common problem occurs when the data has hole outlines or pads in the board outline layer. This suggests to the manufacturer that these holes are required to be non-plated.

But when he compares these locations to the copper layers, it can be seen that these locations have pads and tracks going to them which suggests that these holes require plating. So again the order goes on hold and valuable time is lost. It is important for the designer to double check holes and tracks in the outline and make sure they have corresponding information in the other layers. Notes for the manufacturer are very useful to help alleviate misunderstandings.

ISSUE 3.3

CONFIRM SILKSCREEN CHARACTERS.



Result: Unnecessary delay while the manufacturer asks for clarification.

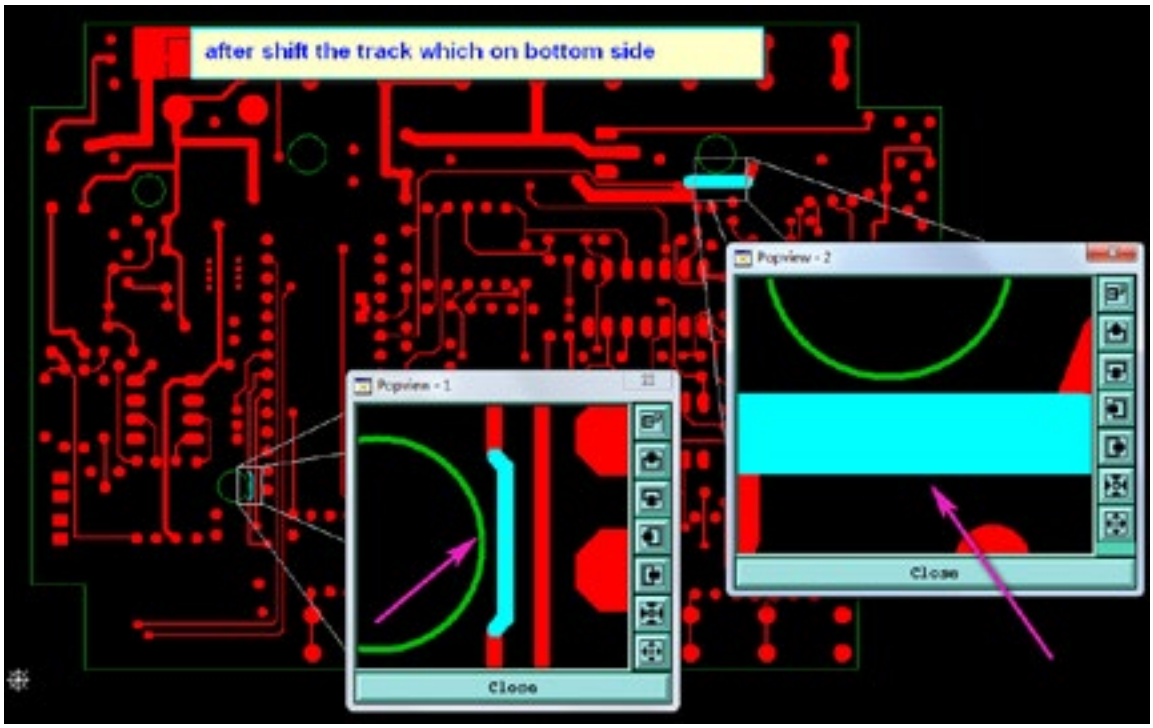
In this example, the customer requested to have top silkscreen on the boards. An extra layer was added that, when viewed, looked like it should be added to the silkscreen layer. Without any instructions the manufacturer had no choice but to hold production and clarify.

ISSUE 4

MANUFACTURER'S SPECIFICATIONS

ISSUE 4.1

NON-PLATED HOLES TOO CLOSE TO THE TRACK.

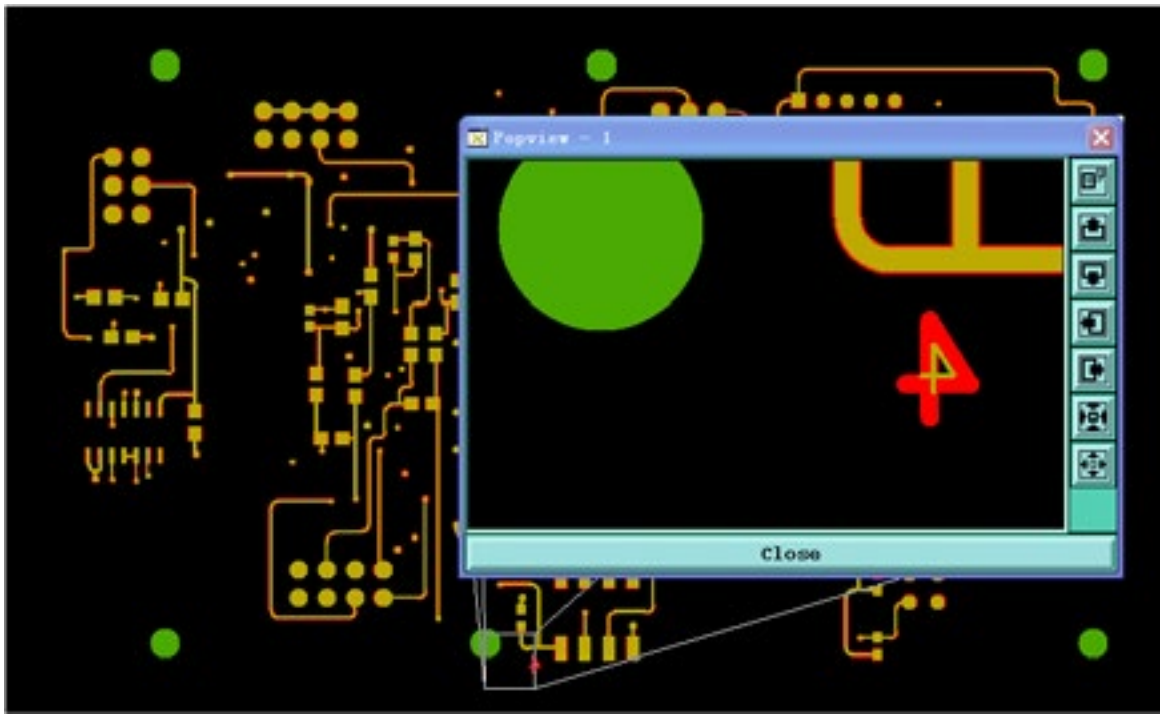


Result: Unnecessary delay while the manufacturer asks for changes.

When designing a PCB, it is important to be familiar with all the manufacturer's minimum criteria. In this example, the PCB designer adhered to all the familiar manufacturing specifications but ignored the minimum gap requirment between tracks and non-plated drills. If no such spec is available, a good approximation is achieved by adding the minimum annular ring requirment for a component hole and the minimum pad to track spacing, and keeping a minimum of that distance between non-plated drills and cut-outs and the nearest tracks.

ISSUE 4.1

ETCH CHARACTERS TOO SMALL.



Result: Potential unnecessary delay while the manufacturer asks for clarification. Unslightly, PCB design.

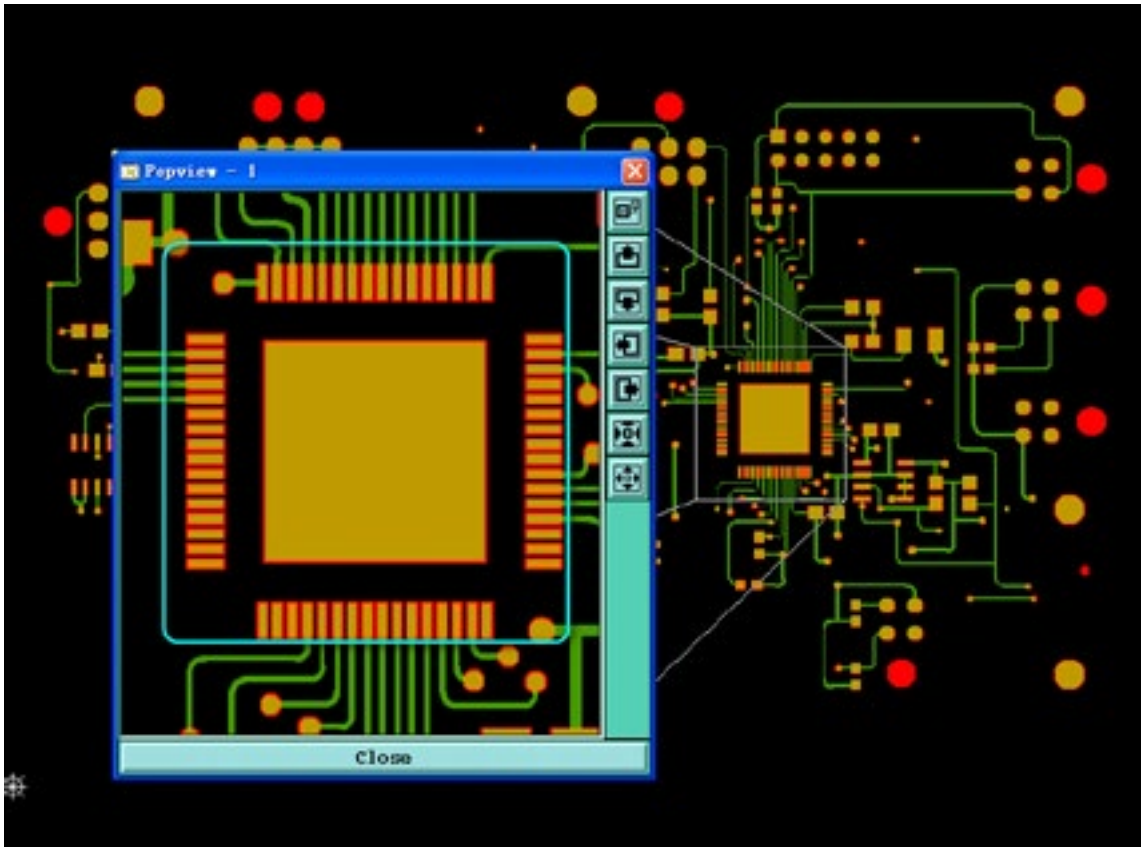
Check what is the smallest possible text size that can be manufactured. Electrically the function of the PCB wont be affected. Text that is too small cannot be clearly read and doesn't properly represent the work you put into your design. It may also result in delays while the manufacturer clarifies.

ISSUE 4.1

COPPER THICKNESS IS 2OZ (75UM) AND SPACE IS 8.7MIL BETWEEN IC PADS.

Result: Unnecessary delay while the manufacturer asks for changes.

Normally, when a manufacturer specifies a minimum track and gap, they are basing that on the standard Cu thickness they provide, generally 1oz or 35um. If you require a board with a heavier copper thickness this may change the manufactuiring specification, so the best advise is to check before hand.



ISSUE 5 - MISSING INFORMATION

ISSUE 5.1

PLACEMENT OF UL LOGO AND DATE CODE.

Result: Unnecessary delay while the manufacturer asks for clarification.

If you make a request that a UL code and a date code are added to your PCBs, please be aware that there are different possible methods and locations for doing this. They could be placed in either the coppers layers, the soldermask layers or possibly added to the silkscreen. You, as the customer, must provide a preference and also specify a location within the board where you would like the information to be placed. Otherwise, add a note to your order that the logos can be placed at the manufacturers discretion.

MINT-TEK

MINT-TEK.COM

sales@mint-tek.com +353 87 239 0096

facebook.com/MintTek/

twitter.com/MintTekCircuits

linkedin.com/company/mint-tek-circuits